# CCS Technical Documentation
# RH-48 Series Transceivers

# System Module

Issue 1 11/2003 Confidential
©2003 Nokia Corporation

## Contents

Transceiver RH-48 ..... 3
Introduction ..... 3
Operational Modes ..... 3
Baseband Module ..... 3
UEM ..... 4
BB-RF Interface Connections ..... 6
UPP ..... 9
NOR Flash Memory and SRAM ..... 10
User Interface Hardware ..... 10
LCD ..... 10
Keyboard ..... 10
Power Key ..... 10
Lights ..... 10
Vibra ..... 11
Audio Hardware ..... 11
Earpiece ..... 11
Microphone ..... 11
MIDI Speaker ..... 11
Audio Amplifier Interface ..... 12
Battery ..... 12
Phone Battery ..... 12
Battery Connector ..... 13
Accessories Interface ..... 13
System connector ..... 13
Charger IF ..... 15
Test Interfaces ..... 16
Production Test Pattern ..... 16
General Information about Testing ..... 18
Phone Operating Modes ..... 18
RF Module ..... 19
Requirements ..... 19
Antenna ..... 19
Transmitter ..... 19
Synthesizer ..... 20
Receiver ..... 22


©2003 Nokia Corporation

# Transceiver RH-48

## Introduction

The RH-48 is available as a CDMA single-band engine (800 MHz CDMA).

## Operational Modes

There are several different operational modes: Modes have different states controlled by the cellular SW. Some examples are:  Idle State (on ACCH), Camping (on DCCH), Scanning, Conversation, No Service Power Save (NSPS) *previously OOR = Out of Range*.

In the **power-off** mode, only the circuits needed for power-up are supplied.

In the **idle** mode, circuits are powered down and only the sleep clock is running.

In the **active** mode, all the circuits are supplied with power, although some parts might be in idle state part of the time.

The **charge** mode is effective in parallel with all previous modes. The charge mode itself consists of two different states, *i.e.* the fast charge and the maintenance mode.

The **local** mode is used for alignment and testing.

## Baseband Module

The core part of the RH-48 baseband module consists of two ASICs — UEM and UPP — and combo memory. The following sections describe these parts.

 ©2003 Nokia Corporation 

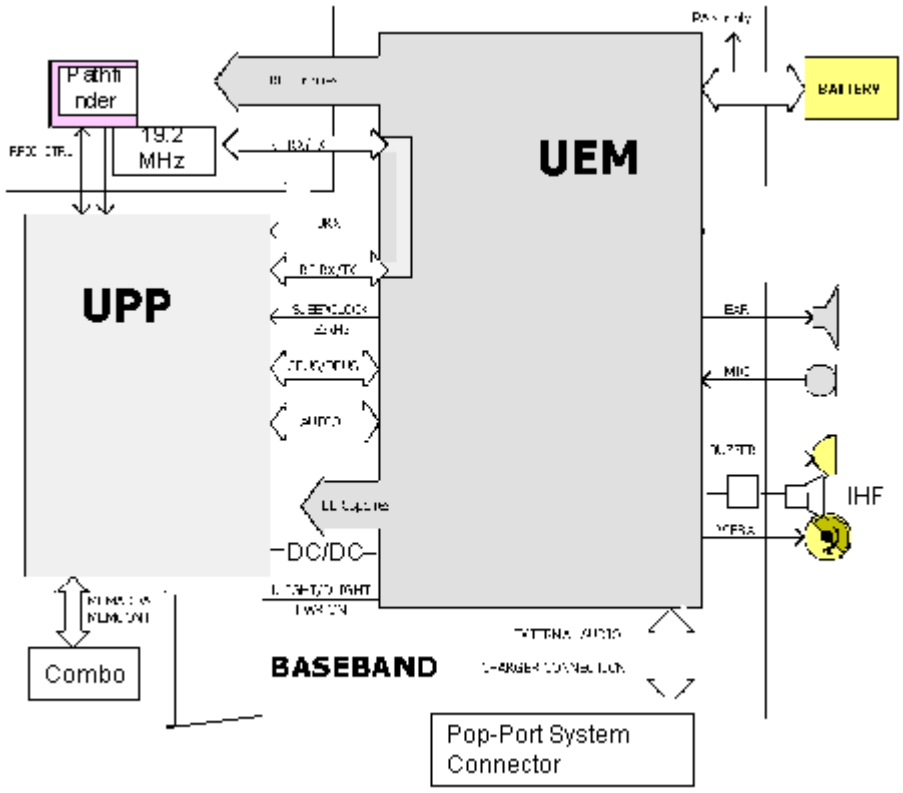



**Figure 1: Baseband module diagram**

## UEM

### UEM Introduction

UEM is the Universal Energy Management IC for DCT4 digital handportable phones. In addition to energy management, it performs all the baseband mixed-signal functions.

Most of UEM pins have 2kV ESD protection. Those signals that are considered to be exposed more easily to ESD have 8kV protection inside UEM. Such signals are all audio signals, headset signals, BSI, Btemp, Fbus, and Mbus signals.

### Regulators

UEM has six regulators for baseband power supplies and seven regulators for RF power supplies. RH-48 has a DC/DC connector to provide power to the UPP VCORE.

Bypass capacitor (1uF) is required for each regulator output to ensure stability.

Reference voltages for regulators require external 1uF capacitors. Vref25RF is reference voltage for VR2 regulator; Vref25BB is reference voltage for VANA, VFLASH1, VFLASH2, VR1 regulators; Vref278 is reference voltage for VR3, VR4, VR5, VR6, VR7 regulators; VrefRF01 is reference voltage for VIO, VCORE, VSIM regulators, and for RF.


©2003 Nokia Corporation

| BB | RF |
|---|---|
| VANA: 2.78V typ 80mA max | VR 1a: 4.75V 12mA max |
| Vflash1: 2.78V typ 70mA max | |
| Vflash2: 2.78V typ 40mA max | VR2: 2.78V 100mA max |
| VSim: 1.8/3.0V 25mA max | VR3: 2.78V 20mA max |
| VIO: 1.8V typ 150mA max | VR4: 2.78V 50mA max |
| Vcore: 1.0-1.8V 100mA max | VR5: 2.78V 50mA max |
| | VR6: 2.78V 50mA max |
| | VR7: 2.78V 45mA max |

VANA regulator supplies internal and external analog circuitry of BB. It is disabled in sleep mode.

Vflash1 regulator supplies LCD and digital parts of UEM ASIC. It is enabled during startup and goes to low Iq-mode in sleep mode.

VIO regulator supplies both external and internal logic circuitries. It is used by LCD, flash, Jedi, Yoda, and UPP. Regulator goes in to low Iq-mode in sleep mode.

VCORE supplies DSP, Core part of UPP. Voltage is programmable and the startup default is 1.5V. Regulator goes to low Iq-mode in sleep mode. VCORE is supplied by DC/DC (the internal regulator is not used).

VR1 regulator (VR1a) uses two LDOs and a charge pump. VR1a is used to bias cellular PA.

VR2 is a linear regulator used to supply Jedi RF ASIC.

VR3 is a linear regulator used by Yoda RF ASIC and VCTCXO circuitry.

VR4 is a linear regulator used by Alfred's LNA RF front end ASIC circuitry.

VR5 is a linear regulator used by Jedi RFIC.

VR6 is a linear regulator used by Yoda RFIC

VR7 is a linear regulator used by synthesizer and VCO circuits on both Jedi and Yoda RFIC

RF Interface

In addition to the RF regulators mentioned, UEM handles the interface between the baseband and the RF section. It provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths, and also A/D and D/A conversions of received and transmitted audio signals to and from the UI section. The UEM supplies the

 ©2003 Nokia Corporation 

analog AFC signal to the RF section according to the UPP DSP digital control. It also converts PA temperature into real data for the DSP. The UPP controls the RFIC through the 3-wire RFIC bus. UPP also provides PDM regulator for RF interface (RX/TX AGC control).

Charging Control

The CHACON block of UEM asics controls charging. Needed functions for charging controls are pwm-controlled battery charging switch, charger-monitoring circuitry, battery voltage monitoring circuitry and RTC supply circuitry for backup battery charging. In addition, external components are needed for EMC protection of the charger input to the baseband module. The DCT4 baseband is designed to electrically support both DCT3 and DCT4 chargers.

Digital Interface

Data transmission between the UEM and the UPP is implemented using two serial connections, DBUS (9.6 MHz) for DSP and CBUS (1.2 MHz in CDMA) for MCU. UEM is a dual-voltage circuit: the digital parts are running from 1.8V and the analog parts are running from 2.78V. Vbat (3.6V) voltage regulators inputs also are used.

Audio Codec

The baseband supports two external microphone inputs and one external earphone output. The inputs can be taken from an internal microphone, from a headset microphone, or from an external microphone signal source through a headset connector. The output for the internal earpiece is a dual-ended type output, and the differential output is capable of driving 4Vpp to the earpiece with a 60 dB minimum signal to total distortion ratio. Input and output signal source selection and gain control is performed inside the UEM ASIC according to control messages from the UPP. Both a buzzer and an external vibra alert control signals are generated by the UEM with separate PWM outputs.

MIDI

The MIDI audio signal generated by the DSP and UEM audio CoDec is routed to the XEAR output of the UEM. An audio amplifier (LM4890) is used to boost enough power for the speaker.

UI Drivers

The vibra, display LED, and keyboard LEDs are driven by open collector output drivers inside UEM. These drivers can generate PWM square wave signals to these devices.

AD Converters

There is an 11-channel analog-to-digital converter in UEM. The AD converters are calibrated in the production line.

## BB-RF Interface Connections

All the signal descriptions and properties in the following tables are valid only for active signals.

 ©2003 Nokia Corporation 

**Table 1: PDM Interface**

| Signal name | From | To | Parameter | Min | Typ | Max | Unit | Function |
|---|---|---|---|---|---|---|---|---|
| RX_IF_AGC | UPP GenIO 9 | Yoda | Voltage Min<br>Max<br>---<br>Clk Rate (1) | 0.0<br>1.75<br>--- | 1.8<br>---<br>9.6 | 0.1<br>1.86<br>---<br>19.2 | V<br><br>---<br>MHz | Controls gain of VGA r in receiver |
| TX_IF_AGC | UPP GenIO 7 | Jedi | Voltage Min<br>Max<br>---<br>Clk Rate (1) | 0.0<br>1.75<br>--- | 1.8<br>---<br>9.6 | 0.1<br>1.86<br>---<br>19.2 | V<br><br>---<br>MHz | Controls gain of VGA in IF VGA |
| TX_RF_AGC | UPP GenIO 26 | Jedi | Voltage Min<br>Max<br>---<br>Clk Rate (3) | 0.0<br>1.75<br>--- | 1.8<br>---<br>9.6 | 0.1<br>1.86<br>---<br>19.2 | V<br><br>---<br>MHz | Controls gain of TX driver |

**Table 2: General I/O Interface**

| Signal name | From | To | Parameter | Input characteristics | Function |
|---|---|---|---|---|---|
| TX_Gate | UPP Gen IO 8 pullup | Jedi and PA Gating Transistors | "0" Transmitter Off<br>"1" Transmitter On<br>Timing Accuracy | 1.38 1.88 V<br>0 0.4 V<br>4 chips, and can be up to a total of 255 chips | Punctures the PA's and the Jedi ASIC<br><br>Digital Into RF |
| D0 | UPP Gen IO 10 | PMIC | Voltage Min<br>Max | 0.4V max<br>1.72V-1.86V | Enable PMIC |
| D1 | UPP Gen IO 13 | PMIC | Voltage Min<br>Max | 0.4V max<br>1.72V-1.86V | Set PMIC output voltage |
| D2 | UPP Gen IO 12 | PMIC | Voltage Min<br>Max | 0.4V max<br>1.72V-1.86V | Set PMIC output voltage |

**Table 3: VCTCXO Interface**

| Signal name | From | To | Parameter | Min | Typ | Max | Unit | Function |
|---|---|---|---|---|---|---|---|---|
| 19.2M_UPP | Yoda | UPP | Frequency<br>---<br>Signal amplitude | ---<br>0.5 | 19.2<br>---<br>1.0 | ---<br>1.5 | MHz<br>---<br>-<br>Vpp | High stability clock signal for logic cir-cuits, AC coupled sinewave. |
| AFC | UEM | VCTCXO | Voltage Min<br>Max<br>---<br>Settling time (4) | 0.0<br>2.4<br>--- | --- | 0.1<br>2.55<br>---<br>0.2 | V<br><br>---<br>ms | Automatic fre-quency control signal for VCTCXO<br>Digital Into RF |

 ©2003 Nokia Corporation 

**Table 4: Regulated Supplies from UEM to RF**

| Signal name | From | To | Parameter | Min | Typ | Max | Unit | Function |
|---|---|---|---|---|---|---|---|---|
| VBAT | Battery | PA & UEM, external driver amps | Voltage<br>----------<br>Current | 3.2<br>-----<br>0 | 3.5<br>------ | 5.1<br>------<br>2A peak | V<br>------ | Battery supply. Lower limit is to guarantee regulator PSRR |
| VR1A | UEM | PA Vref | Voltage<br>----------<br>Current | 4.6<br>------<br>0 | 4.75<br>------<br>4 | 4.9<br>------<br>5 | V<br>------<br>mA | Charge pump + linear regulator. |
| VR2 | UEM | Jedi | Voltage<br>----------<br>Current | 2.70<br>------ | 2.78<br>------ | 2.86<br>------<br>100 | V<br>------<br>mA | Linear regulator |
| VR3 | UEM | VCTCXO, Yoda | Voltage<br>----------<br>Current | 2.70<br>------ | 2.78<br>------ | 2.8<br>------<br>20 | V<br>------<br>mA | Low noise linear regulator for VCTCXO |
| VR4 | UEM | Alfred | Voltage<br>----------<br>Current | 2.70<br>------ | 2.78<br>------ | | V<br>------<br>mA | Low lq linear regulator |
| VR5 | UEM | Jedi | Voltage<br>----------<br>Current | 2.70<br>------ | 2.78<br>------ | | V<br>------<br>mA | Low lq linear regulator |
| VR6 | UEM | Yoda | Voltage<br>----------<br>Current | 2.70<br>------ | 2.78<br>------ | | V<br>------<br>mA | Low lq linear regulator |
| VR7 | UEM | Jedi | Voltage<br>----------<br>Current | 2.70<br>------ | 2.78<br>------ | | V<br>------<br>mA | Low noise linear regulator for synthesizer |
| VIO | UEM | Jedi, Yoda | Voltage | 1.70 | 1.8 | 1.88<br>-------<br>50 | V<br>------<br>mA | Supply for RF-BB digital signal interface and some digital parts of RF |
| Vref_rf01 | UEM | Yoda | Voltage | 1.334 | 1.35 | 1.366 | V | Voltage refer for Yoda I/or de-modulator |

**Table 5: Slow A/D Converters**

| Signal name | From | To | Parameter | Min | Typ | Max | Unit | Function |
|---|---|---|---|---|---|---|---|---|
| PA_TEMP | Thermistor | UEM | Input voltage range | 0 | | 2.78 | V | PA temperature sensor output voltage<br>Analog Out of RF |
| PWROUT | Jedi | UEM | Input voltage range | 0 | | 2.78 | V | Buffered output of TX output detector |


©2003 Nokia Corporation Confidential

**Table 6: RF-BB Analog Signals**

| Signal name | From | To | Parameter | Min | Typ | Max | Unit | Function |
|---|---|---|---|---|---|---|---|---|
| RX_IP_RF<br>RX_IN_RF<br>RX_QP_RF<br>RX_QN_RF | Yoda | UEM | Differential voltage swing (static)<br>---<br>DC level<br>---<br>Input Bandwidth | 0.3<br>---<br>1.3<br>--- | 0.5<br>---<br>1.35<br>--- | 1.0<br>---<br>1.4<br>---<br>615 | Vpp<br>---<br>V<br>---<br>kHz | Differential in-phase and quadrature RX baseband signal<br><br>Analog Out of RF |
| TX_IP_RF<br>TX_IN_RF<br>TX_QP_RF<br>TX_QN_RF | UEM | Jedi | Differential voltage swing (static)<br>---<br>DC level<br>---<br>-3 dB Bandwidth | 0.4<br>---<br>1.65<br>---<br>650 | 0.8<br>---<br>1.7<br>--- | 1.2<br>---<br>1.75<br>---<br>1950 | Vpp<br>---<br>V<br>---<br>kHz | Differential quadrature phase TX baseband signal for RF modulator<br><br>Analog into RF |

**Table 7: RFIC Control**

| Signal name | From | To | Parameter | Min | Typ | Max | Unit | Function |
|---|---|---|---|---|---|---|---|---|
| RF_BUS_CLK<br>RF_BUS_DATA<br>RF_BUS_EN1X | UPP | Jedi, Yoda | High-level input voltage, $V_{IH}$<br><br>Low-level input voltage, $V_{IL}$<br><br>High-level output voltage, $V_{OH}$<br><br>Low-level output voltage, $V_{OL}$<br><br>Clock | 1.72<br><br><br><br>1.72<br><br><br><br> | 1.8<br><br><br><br>1.8<br><br><br><br>9.6 | 1.86<br><br>0.4<br><br>1.86<br><br>0.4<br><br> | V<br><br>V<br><br>V<br><br>V<br><br>MHz | Serial Clock = Digital Into RF<br><br>Bidirectional Serial Date = Digital I/O<br><br>Latch enable for Jedi and Yoda = Digital Into RF |

## UPP

### Introduction

RH-48 uses UPP8Mv3.5 ASIC. The RAM size is 8Mbit. The UPP ASIC is designed to operate in a DCT4 engine, and is designed as part of the DCT4 common baseband task force. The DCT4 processor architecture consists of both DSP and MCU processors.

### Blocks

UPP is internally partitioned into two main parts: the Brain and the Body.

The Brain consists of the Processor and Memory System (*i.e.*, Processor cores, Mega-cells, internal memories, peripherals, and external memory interface). The following blocks are included: the DSP Subsystem (DSPSS), the MCU Subsystem (MCUSS), the emulation control EMUCtl, the program/data RAM PDRAM, and the Brain Peripherals–subsystem (BrainPer).

 ©2003 Nokia Corporation 

The Body consists of the NMP custom cellular logic functions. These contain all interfaces and functions needed for interfacing with other DCT4 baseband and RF parts. It includes the following sub-blocks: MFI, SCU, CTSI, RxModem, AccIF, UIF, Coder, GPRSCip, BodyIF, SIMIF, PUP, and CDMA (Corona).

### NOR Flash Memory and SRAM

This device is a 128Mbit Muxed Burst Multi Bank Flash and 8Mbit Muxed fCMOS SRAM combined in a Multi Chip Package Memory.

The 128Mbit Flash memory is organized as 8M x 16 bit and 8Mbit SRAM is organized as 512K x 16 bit. The memory architecture of flash memory is designed to divide its memory arrays into 263 blocks and this provides highly flexible erase and program capability. This device is capable of reading data from one bank while programming or erasing in the other banks with multi-bank organization.

The Flash memory performs a program operation in units of 16 bits (Word) and erases in units of a block. Single or multiple blocks can be erased. The block erase operation is completed for typically 0.7 sec.

The 8Mbit Muxed fCMOS SRAM supports low data retention voltage for battery backup operation with low data retention current.

## User Interface Hardware

### LCD

The RH-48 uses a 128 x 128 color display.

LCD is controlled by UI SW and control signals.

### Keyboard

RH-48 keyboard design is 4-way scroll, with navigation keys, two soft keys, and 12 number keys. The PWR key is located on top.

### Power Key

All signals for keyboard are coming from UPP asic except pwr key signal which is connected directly to UEM. Pressing of pwr key is detected so that switch of pwr key connects PWONX is of UEM to GND and creates an interrupt.

### Lights

Introduction

RH-48 has six white LEDs for keyboard lighting purposes. The LEDs for the Display are integrated into the Display Module.

Interfaces

Display lighting and keyboard lights are controlled by UEM Klight signal (8-bit register DriverPWMR, bits 7...4). Klight output is Pulse Width Modulation (PWM) signal, which is

 ©2003 Nokia Corporation Confidential 

used to control average current going through LEDs. A step-up converter and a constant current source is used to ensure that the LEDs provide uniform intensity and color.

### Vibra

Introduction

Vibra is located on the D-cover and is connected by spring connectors on the PWB. It is located in the bottom of the engine.

Interfaces

Vibra is controlled by pwm signal VIBRA from UEM. This signal allows control of both frequency and pulse width of signal. Pulse width is used to control current when battery voltage changes. Frequency control searches for optimum frequency to ensure silent and efficient vibrating.

| Parameter | Requirement | Unit |
|---|---|---|
| Rated DC voltage | 1.3 | V |
| Rated speed | 9500 ± 3000 | rpm |
| Rated current | 115 ± 20 | mA |
| Starting current | 150 ± 20 | mA |
| Armature resistant | 8.6 | ohm |
| Rated DC voltage available | 1.2 to 1.7 | V |
| Starting DC voltage | min 1.2 | V |

## Audio Hardware

### Earpiece

The 13 mm speaker capsule that is used in DCT3 products also is used in . The speaker is dynamical—very sensitive, and capable of producing relatively high sound pressure at low frequencies. The speaker capsule and surrounding mechanics comprise the earpiece.

### Microphone

The microphone is an electric microphone with omnidirectional polar pattern. It consists of an electrically polarized membrane and a metal electrode, which form a capacitor. Air pressure changes (*i.e.*, sound) move the membrane, which causes voltage changes across the capacitor. Since the capacitance is typically 2 pF, a FET buffer is needed inside the microphone capsule for the signal generated by the capacitor. The microphone needs bias voltage as a result of the FET.

### MIDI Speaker

Musical Instrument Digital Interface (MIDI) defines the data interchange format. By implementing MIDI engine, enriched sound effect will be achieved, which includes: ringing tones, UI event sounds, and music for games and entertainment.

 ©2003 Nokia Corporation 

The MIDI data stream is a unidirectional, asynchronous bit stream at maximum 31.25 kbits/sec. with 10 bits transmitted per byte (a start bit, 8 data bits, and one stop bit).

MIDI data includes two categories of signals: MIDI tones and Alerting Tones. Both are generated from DSP and send to the MIDI speaker.

### Audio Amplifier Interface

From audio hardware point, since the audio output from UEM is not strong enough to produce enough power for the speaker, an audio amplifier is required.

The MIDI audio signal generated by the DSP and UEM audio CoDec is routed to the XEAR output of the UEM. An audio amplifier is used to boost enough power for the speaker. GENIO (28) is used to enable/disable the audio amplifier as needed.

## Battery

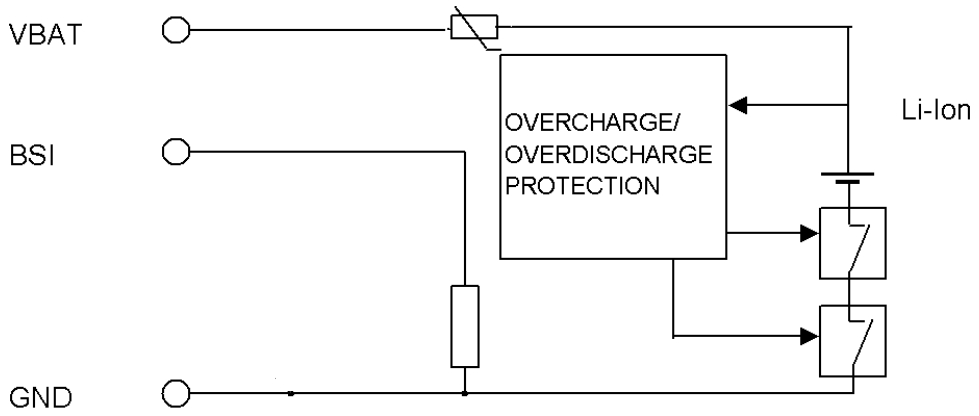
### Phone Battery

Introduction

An 850 mAh Li-ion battery (BL-5C) is standard in RH-48.

Interface

The battery block contains  BSI resistors for battery identification. The BSI fixed resistor value indicates the chemistry and default capacity of a battery. This resistor is connected to the BSI pin of battery connector. Phone has pull-up resistors (R202) for these lines so that they can be read by A/D inputs in the phone (see the following figure). There also are spark caps in the BSI line to prevent ESD.




Battery has internal protection for overvoltage and overcurrent.


©2003 Nokia Corporation

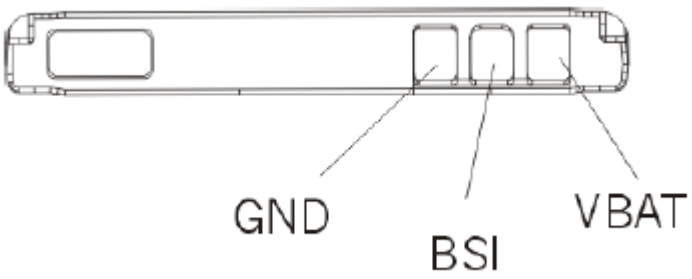



Figure 2: Battery pack pin order

### Battery Connector

RH-48 uses a spring-type battery connector. This ensures a more reliable connection between the battery and PWB.

| # | Signal name | Connected from - to | Batt I/0 | Signal properties A/D-levels-freq./ timing | Description/ Notes |
|---|---|---|---|---|---|
| 1 | VBAT | (+) (batt.) | VBAT | I/O | Vbat |
| 2 | BSI | BSI (batt.) | UEM | Out | Ana |
| 3 | GND | GND | GND | | Gnd |

## Accessories Interface

### System connector

Introduction

RH-48 uses the Tomahawk accessories via the Tomahawk connector.

Interface

Tomahawk bottom connector consists of charging plug socket and Tomahawk System connector (see figures that follow). Minimum configuration of Tomahawk interface includes charging, mono audio, power out, ACI and Fbus. USB and stereo audio out are optional.

Tomahawk system connector includes:

- Charging

  Pads for 2 -wire charging in cradles

- Audio

  2 -wire fully differential output audio

 ©2003 Nokia Corporation 

2-wire differential mic input

- Power out

  2.78V 70 mA output to accessories

- Detection/controlling

  ACI

  Point to point bi-directional data line

- Fbus

  Standard Fbus

  AT command mode (Nokia Serial Bus)

  Phonet message mode

  Fast Fbus, fast data bus to add on modules

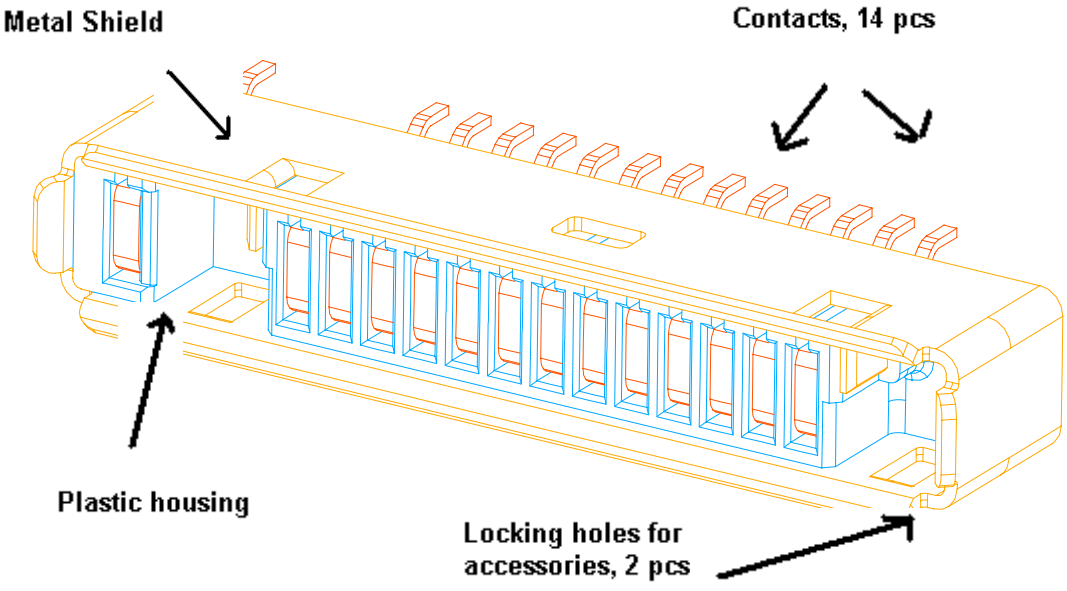



**Figure 3: Tomahawk system connector**


©2003 Nokia Corporation

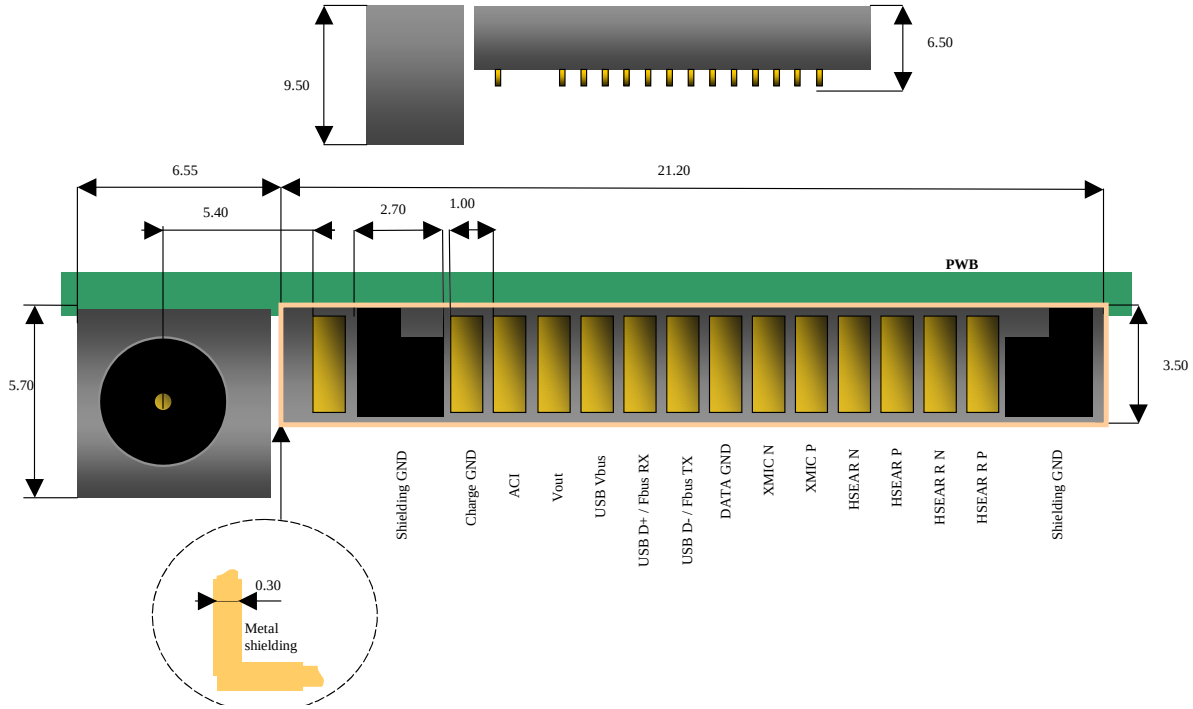



**Figure 4: Mechanical dimensions and signals of Tomahawk bottom connectors**

An accessory is detected by the ACI-line. All accessories will generate interrupt while inserted or removed from the phones Tomahawk system connector. Insertion of an accessory will generate HEADINT interrupt by pulling ACI line down. Vout is enabled by UPP. The MBUS line is connected to HEADINT line. If HEADINT interrupt from low to high transition occurs within 20msec a more advanced accessory is connected else a basic headset is connected.

## Charger IF

### Introduction

The charger connection is implemented through the bottom connector. DCT-4 bottom connector supports charging with both plug chargers and desktop stand chargers.

There are three signals for charging. Charger gnd pin is used for both desktop and for plug chargers as well as charger voltage. PWM control line, which is needed for 3-wire chargers, is connected directly to gnd in module PWB so the RH-48 engine doesn't provide any PWM control to chargers. Charging controlling is done inside UEM by switching UEM internal charger switch on/off.

### Interface

The fuse (F100) protects from high currents (e.g. , when broken or pirate chargers are used). L100 protects engine from RF noises that may occur in charging cable. V100 protects UEM ASIC from reverse-polarity charging and from high charging voltage. C106 is also used for ESD and EMC protection.

## Test Interfaces

### Production Test Pattern

Interface for RH-48 production testing is 5-pin pad layout in BB area (see figure below). Production tester connects to these pads by using spring connectors. Interface includes MBUS, USRX, FBUSTX, VPP, and GND signals. Pad size is 1.7mm. The same pads also are used for AS test equipment such as module jig and service cable.

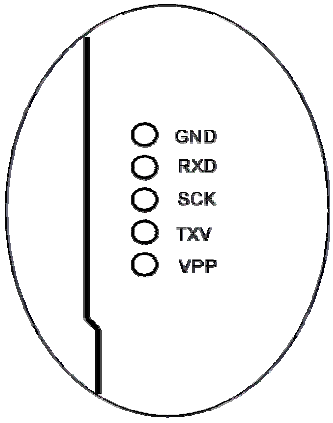



**Figure 5: 5-pin layout in BB area**


©2003 Nokia Corporation

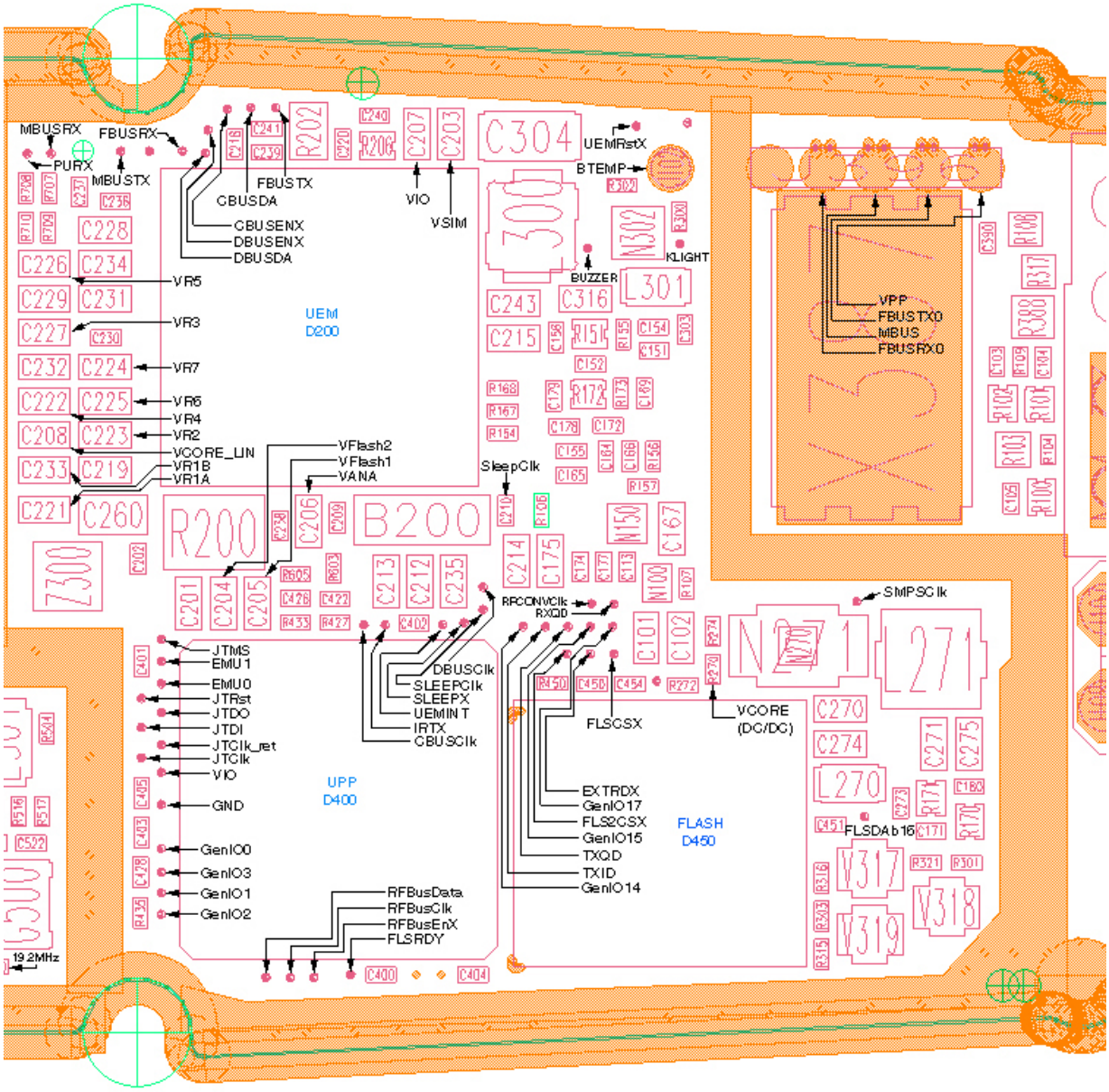



**Figure 6: RH-48** BB test points, regulators, and BB ASICs

 ©2003 Nokia Corporation 

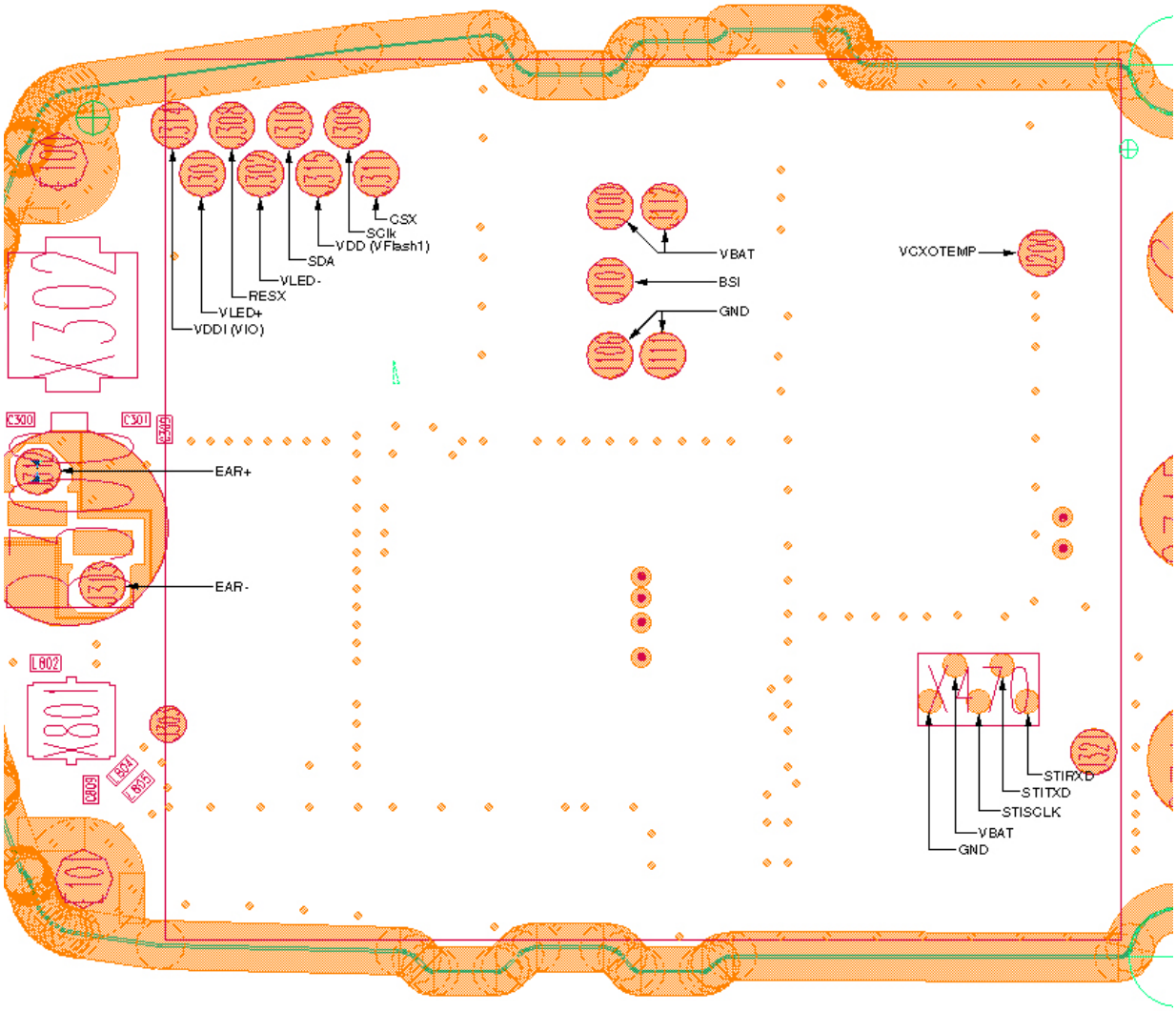



**Figure 7: RH-48 BB test points, regulators, and BB ASICs**

## General Information about Testing

### Phone Operating Modes

The phone has three different modes for test/repair. Modes can be selected with suitable resistors connected to BSI- lines as follows:

| Mode | BSI- resistor | Remarks |
|---|---|---|
| Normal | 75k | |
| Local | 3.3k | |
| Test | 6.8k | Recommended with baseband testing. Similar to Local mode, but making a phone call is possible. |


©2003 Nokia Corporation

The MCU software enters automatically to Local or Test mode at start-up if corresponding resistors are connected.

*Note: Baseband doesn't wake up automatically when the battery voltage is connected (Normal mode).*

## RF Module

### Requirements

RH-48 supports CDMA 800 MHz as described in:

- IS2000-2-A Physical Layer Standard for cdma2000 Spread Spectrum Systems; and
- IS-98D (Draft 4) Recommended Minimum Performance Standard for Spread Spectrum Mobile Stations.

### Antenna

An internal antenna is used.

### Transmitter

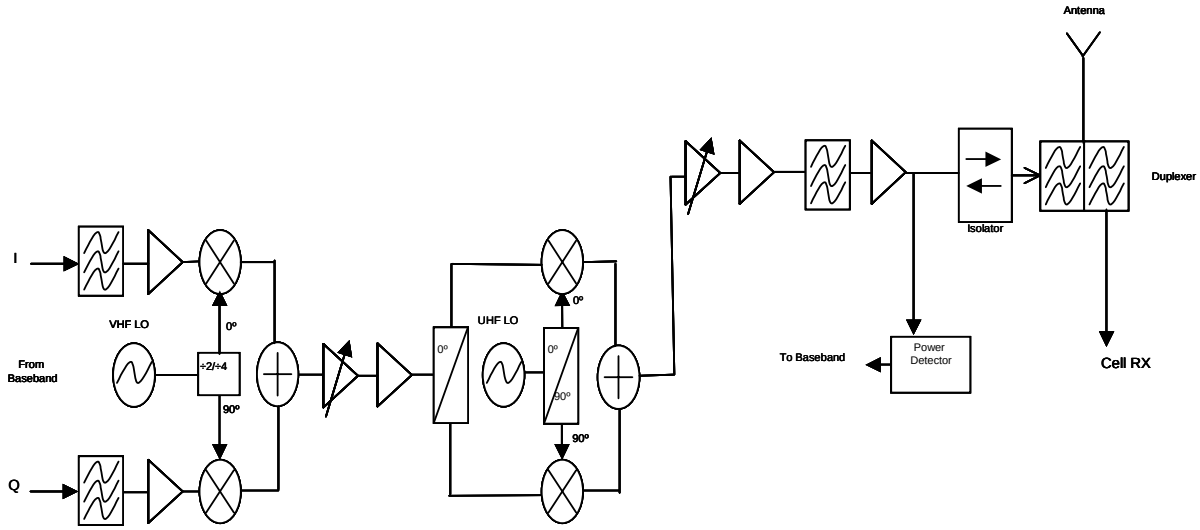



**Figure 8: RF transmitter block diagram**

The transmit chain up to the RF driver stage is integrated into one transmit-integrated circuit called Jedi, with external power amplifiers (PA). The channel spacing is 30 kHz.

All data transmitted on the channel is convolutionally encoded and block-interleaved. Modulation is 64-ary orthogonal (RC1 and RC2) and direct sequence spread by a quadrature pair of PN sequences at a fixed chip rate. The data is filtered, O-QPSK modulated and up-converted to the appropriate transmission frequency. RC3 and RC4 use HPSK modulation at data rates up to 153.6 kBPS (RC3) and 115.2 kBPS (RC4).

The baseband I/Q signals are converted to IF frequency in the I/Q modulator by Quadrature mixing. The modulated IF signals go through a variable gain amplifier (IF AGC) and then are routed to the Cell TX path. The path consists of an upconverter and a variable

gain RF amplifier. The IF signal is converted up to RF with a differential output upconverter and then fed to the RF amplifier. The RF amplifier has variable gain capability (RF AGC) with up to 40 dB of dynamic gain control.

The output of the Cell RF amplifier of Jedi is connected to an RF filter to reject TX noise in the RX band.

The output of the RF filter is connected to the PA. Out of the PA is an isolator, then antenna.

**Synthesizer**

Refer to the following figure for a block diagram that illustrates all three synthesizers and how they interconnect in the system.

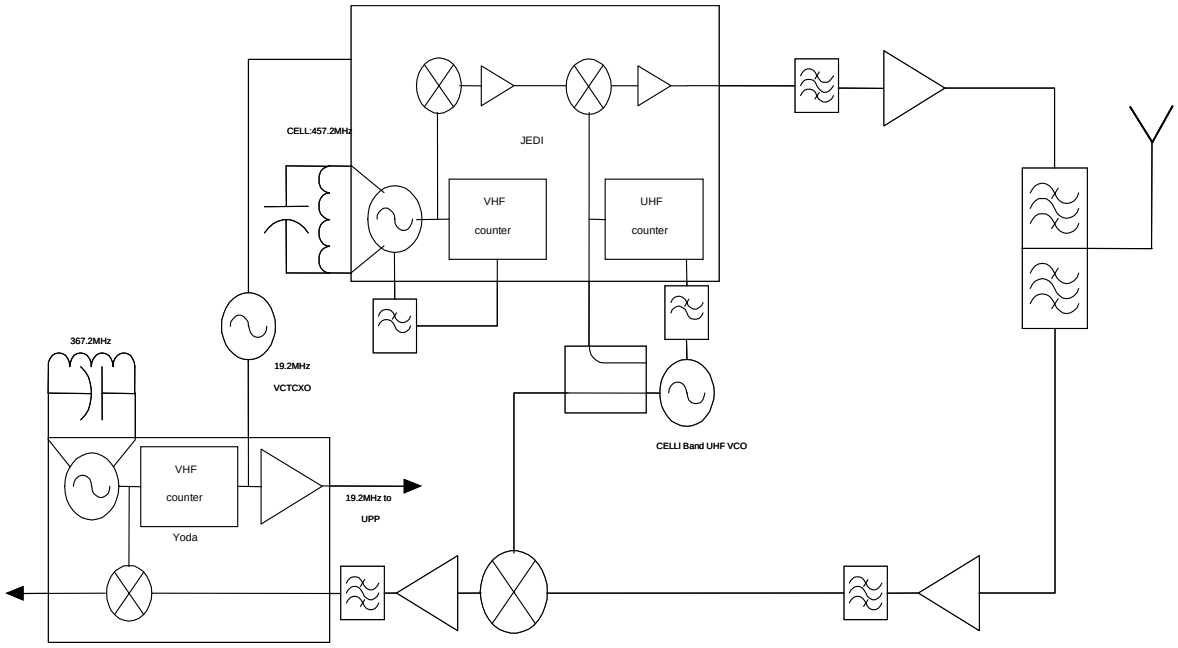



**Figure 9: Synthesizer system block diagram**

1st TX VHF LO Synthesizer (Jedi)

The TX VHF Synthesizer is integrated within the Jedi RFIC and generates the LO signals for the IQ-modulator in Jedi. The synthesizer has an internal VCO with an external resonator. The VCO operates at two times the CELL IF frequencies. A band-switch signal, VCO_Band, is used to shift the center frequency of the external resonator.

The synthesizer is a dual-modulus prescaler type, and utilizes a phase detector with a charge pump that sinks or sources currents, depending on the phase difference between the detector input signals. The width of the pulses depends on the phase difference between the signals at input of the phase detector. The main divider, auxiliary divider, and reference divider are programmable through the serial interface to Jedi.

2nd RX VHF LO Synthesizer (Yoda)

The RX VHF Synthesizer is integrated within the Yoda RFIC and generates the LO signals for the IQ demodulator in Yoda. The synthesizer has an internal VCO with an external

resonator. The VCO operates at two times the common 183.6 MHz RX IF frequency. A band-switch signal, Band_Sel, is used to select the band of operation for the UHF VCO.

The synthesizer is a dual-modulus prescaler type, and utilizes a phase detector with a charge pump that signals or sources currents, depending upon the phase difference between the detector input signals. The width of the pulses depends on the phase difference between the signals at input of the phase detector. The main divider, auxiliary divider, and reference divider are programmable through the serial interface to Yoda.

The RX VHF Synthesizer generates 367.2 MHz.

VCTCXO - System Reference Oscillator

The VCTCXO provides the frequency reference for all the synthesizers. It is a voltage-controlled, temperature-compensated, 19.2MHz crystal oscillator that can be pulled over a small range of its output frequency. This allows for an AFC function to be implemented for any frequency accuracy requirements. This is done by DSP processing of received I/Q signals.

Closed loop AFC operation allows very close frequency tracking of the base station to be done in CDMA mode. This will enable the unit to track out aging effects and give the required center frequency accuracy in cellular band.

The most practical way of clock distribution is driving all three chips (UHF PLL, Yoda, and Jedi) directly from the VCTCXO. An internal buffer is used to drive the UPP in order to isolate the UPP's digital noise from the VCTCXO, which prevents contamination of the 19.2 MHz reference onto the PLL chips of the system. Since the VCTCXO output is a sine-wave, such clock distribution will not cause any clock signal integrity problems, even for relatively long traces (what might occur in case of a digital square waveform with fast transition times). The VCTCXO output is AC, coupled to Yoda, Jedi, UHF PLL, and the digital ASICs (see the following figure) to eliminate DC incompatibility between those pins.

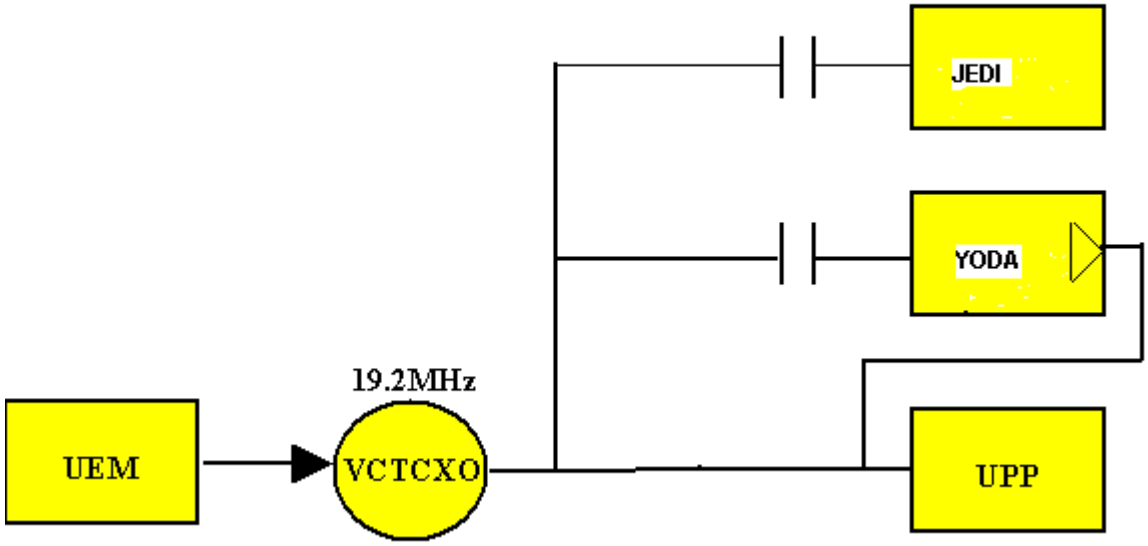



Figure 10: VCTCXO clock distribution

## Receiver

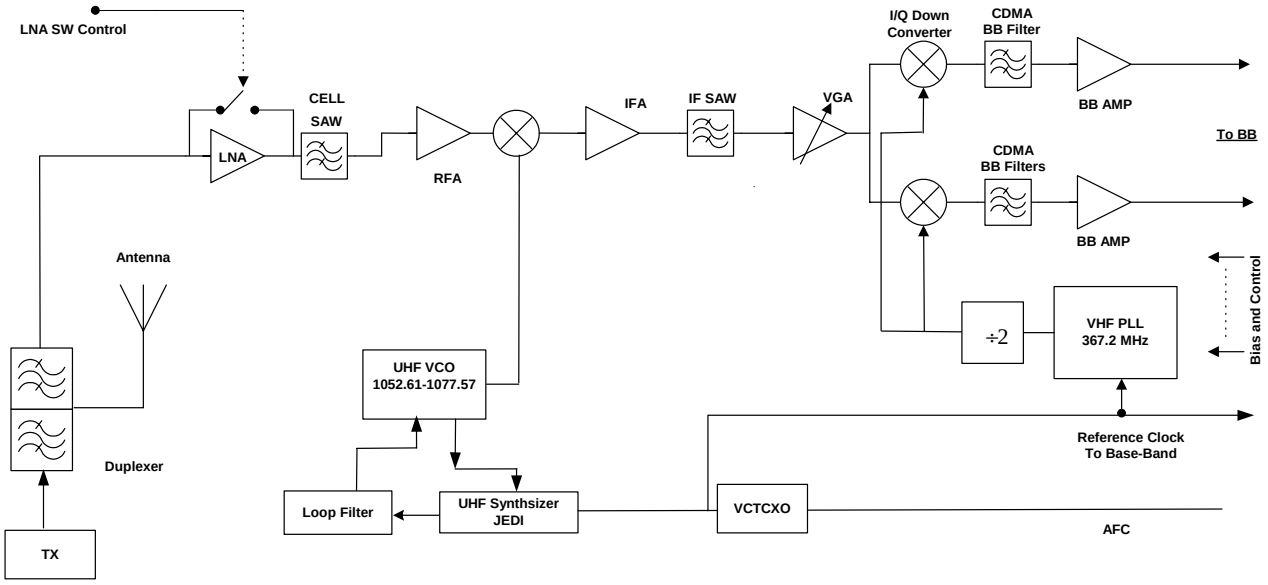



**Figure 11: Receiver block diagram**

The receiver is a dual conversion I/Q receiver with a first IF of 183.6 MHz. The front-end RFIC (Alfred) contains a low noise amplifier (LNA), a radio frequency amplifier (RFA), a down-converter, an intermediate frequency amplifier (IFA), and a local oscillator amplifier (LOA). Between the LNA and the RFA is a bandpass filter which will reject out-of-band spurious and act as image rejection. The IF filter is between the Alfred IC and the Yoda IC. The purpose of this filter is to guarantee rejection in adjacent and alternate channels.

The RX IF ASIC Yoda is used to convert the IF down to baseband I and Q. The ASIC contains a VGA section, IQ demodulator, and baseband filters (BBFIL) for CDMA. Fix gain baseband amplifier (BBAMP), and RX VHF PLL. The I/Q BB signals are output to UEM chip for analog-to-digital conversion and further signal processing.


©2003 Nokia Corporation